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On the mechanism of current-transport in Cu/CdS/SnO_2/In–Ga structures

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ABSTRACT

The structural and optical properties of CdS films deposited by evaporation were investigated. X-ray diffraction study showed that CdS films were polycrystalline in nature with zinc-blende structure and a strong (1 1 1) texture. The study has been made on the behavior of Cu/n-CdS thin film junction on SnO_2 coated glass substrate grown using thermal evaporation method. The forward bias current–voltage (I–V) characteristics of Cu/CdS/SnO_2/In–Ga structures have been investigated in the temperature range of 130–325 K. The semi-logarithmic ln$I$–V characteristics based on the Thermionic emission (TE) mechanism showed a decrease in the ideality factor (n) and an increase in the zero-bias barrier height (Φ_{Bo}) with the increasing temperature. The values of n and Φ_{Bo} change from 8.98 and 0.29 eV (at 130 K) to 3.42 and 0.72 eV (at 325 K), respectively. The conventional Richardson plot of the $\ln(I_o/T^2)$ vs q/kT shows nonlinear behavior. The forward bias current I is found to be proportional to $I_o(T)\exp(AV)$, where A is the slope of $\ln(I)$–V plot and almost independent of the applied bias voltage and temperature, and $I_o(T)$ is relatively a weak function of temperature. These results indicate that the mechanism of charge transport in the SnO_2/CdS/Cu structure in the whole temperature range is performed by tunneling among interface states/traps or dislocations intersecting the space-charge region. In addition, voltage dependent values of resistance (R_i) were obtained from forward and reverse bias I–V characteristics by using Ohm's law for each temperature level.

1. Introduction

Thin oxide (SnO_2) film is technologically important material and it has a wide band gap of 3.6 eV at 300 K. Two of the main reasons for the interest in this material are the high transparency in the visible region and high conductivity. SnO_2 has been widely used as gas sensors, photocatalysts, electrodes of dye-sensitized solar cells (DSSCs), antistatic coatings, and so on [1,2]. This interfacial oxide layer (SnO_2) may have a strong influence on the device characteristics. Cadmium sulfide (CdS) film of the II–VI group is generally used as a wide band gap 2.42 eV semiconductor. CdS is one of the best materials for the fabrication of high efficiency polycrystalline thin film solar cells, either based on cadmium telluride or copper indium diselenide (CIS) [3–5]. On the other hand, the Cu–CdS bilayer systems are used for the preparation of metal-coated semiconductor nanocrystals which are of great interest for the fabrication of optical and electroluminescent devices [5,6]. In general, the CdS semiconductor has n-type conductivity. Donor centers, which are formed in CdS during growth, were attributed to the native point defects (vacancies of the sulfur sub-lattice, the interstitial cadmium atoms, etc.) caused by deviation of CdS composition from the stoichiometry. Recently, semiconductor nanostructures have gained considerable importance because of their unusual optical, electrical and device applications [7–11].

The current-transport/conduction mechanisms in semiconductor devices such as metal–semiconductor (MS), metal–insulator–semiconductor (MIS) and solar cells are dependent on various parameters, such as the process of surface preparation, formation of barrier height (BH) between the metal and semiconductor and its homogeneity, impurity concentration of semiconductor, density of interface states/traps or dislocations, series resistance (R_s) of device, device temperature and applied bias voltage. The current–voltage–temperature (I–V–T) and capacitance–voltage–temperature (C–V–T) characteristics of these devices have been extensively studied and reported in the literature for more than four decades because of simplicity in the fabrication [12–30]. In these devices, different current-transport mechanisms may dominate the others at a certain temperature and voltage regions, such as thermionic emission (TE), thermionic-field emission (TFE), field emission (FE), recombination tunneling via interface states or dislocations, minority carrier injection, recombination and multi-step tunneling. On the other hand, a simultaneous contribution from two or more mechanisms could also be possible.

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Recently, there are a lot of studies in the literature about current-transport mechanisms of MS, MIS and solar cells [19–21,31–34]. Among them, Kar et al. [31], Cao et al. [32] and Özdemir et al. [19] presented very interesting studies, where the results indicated the likelihood of a primary current-transport mechanism to be multistep tunneling and defect assisted tunneling instead of TE, respectively. Evstropov et al. [33], Balyaev et al. [34], Arslan et al. [20] and Bengi et al. [21] showed that the current flow in the III–V heterojunctions is generally governed by multistep tunneling with the involvement of dislocations even at room temperature and with low doping concentrations. They demonstrated that an excess tunnel current could be attributed to dislocations. A model of tunneling through a space-charge region (SCR) along a dislocation line is suggested [33].

It is well known the analysis of the forward bias *I–V* characteristics of these devices measured only at room temperature does not give a detailed information about the current-transport mechanisms and the nature of the barrier height formed between metal and semiconductor. On the other hand, the forward-bias *I–V* characteristics in a wide temperature range enable us to understand the different aspects of the current-transport mechanism and barrier formation. Therefore, the first aim of the present study is to investigate the current-transport mechanism in the forward-biased on the Cu/CdS/SnO_2/In–Ga structures with a high dislocation compared with the literature in a wide temperature range (130–325 K). The second aim is to achieve a better understanding of the temperature dependence of R_s and its effect on the *I–V* characteristics in the wide range applied bias voltages.

2. Experimental

The n-type CdS thin films were deposited by vacuum evaporation in a quasi-closed volume on soda-lime glass and SnO_2 coated glass substrates (30–60 Ω/sq, from Aldrich Chemical Company, USA) using high purity CdS polycrystalline powder (99.99%, from Aldrich Chemical Company, USA) as the source materials. The cross-sectional view of the evaporation apparatus is given in Fig. 1. The substrate holder was fixed at a distance of 5 cm above the quartz filter and the distance between quartz filter and source materials was 5 cm. Substrates were clamp-mounted onto the holder face down and they had direct view of the quartz filter. Source and substrate holder temperatures were monitored and controlled separately using a K-type thermocouple during evaporation. After loading the source material into the source bottle, the chamber was closed and allowed to evacuate using a rotary and diffusion pump. The chamber was evacuated to 3×10^{-2} Pa during evaporation. The first heater was able to adjust its temperature 500 °C. Evaporation rate of the source material was controlled by keeping the source temperature within the range of 600 °C and kept relatively low to avoid substrate heating. The deposition rate was 3 nm/s [10].

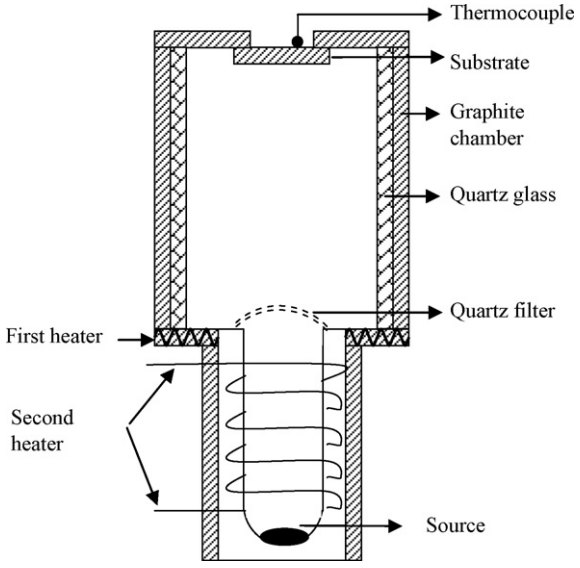

Fig. 1. A cross-sectional view of the thermal evaporation apparatus.

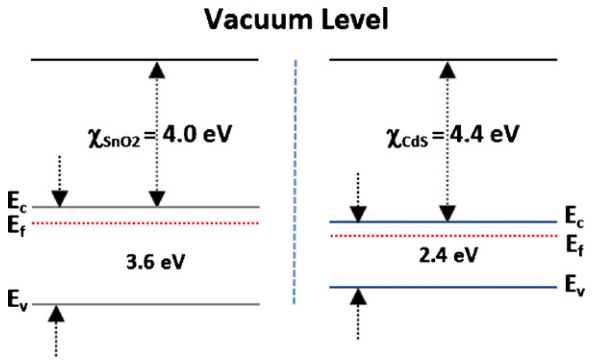

Fig. 2. The energy-band diagram of the SnO_2 and CdS before contact.

After CdS thin films coated on SnO_2, SnO_2/CdS structures were annealed at temperature of 300 °C for 1 h in vacuum in order to improve the back contact. The resistivity and the carrier concentration of CdS films were determined by Van Der Pauw and Hall effect measurements which were carried out at room temperature. The values of resistivity and charge carrier concentration for the as-grown n-type CdS films obtained on the glass substrate with a thickness of about 2 μm were found to be 1.8×10^4 Ω cm and $n = 1.8 \times 10^{13}$ cm^{-3}, respectively. The thicknesses of CdS thin films were measured by PHE 102 Spectroscopic Ellipsometry. Cu element was deposited onto CdS thin films by using a vacuum evaporation method. Circular Cu Schottky/rectifier contacts with 2 mm diameter were deposited on the upper surface of the CdS films by vacuum evaporation system. The ohmic contacts of SnO_2 coated glass were made of indium–gallium as shown in the inset of Fig. 4(a). In order to obtain low resistivity ohmic contact, we used In–Ga alloy. The soldering material is In–Ga mixture which is prepared by using equal amounts of In and Ga at relatively low temperature at about 150 °C. The samples were mounted on a copper holder with the help of silver dag and the electrical contacts were made to the upper electrodes by the used of tiny silver coated wires with silver paste. Fig. 2 shows the energy band diagram of the SnO_2 and CdS before contact. SnO_2 and CdS have a bulk electron affinity (χ) of about 4.0 and 4.4 eV, respectively. The electron affinity does not depend on doping concentration (donor or acceptor) and it defined as the energy difference of an electron between the vacuum level and top of the conductance band [35,36].

X-ray diffraction (XRD) data was collected using a Rigaku D/Max-IIIC diffractometer with CuK_α radiation over the range of $2\theta = 20°$–$60°$ at room temperature. The temperature dependence *I–V* measurements were performed using a Keithley 2400 source meter. The *I–V* measurements of the Cu/CdS/SnO_2/In–Ga structures were measured in the temperature range of 130–325 K using a temperature controlled Janis vpf-475 cryostat, which enables us to make measurements in the temperature range of 77–450 K. The sample temperature was always monitored using a copper-constant and thermocouple close to the sample and measured with a dmm/scanner Keithley model 199 and a Lake Shore model 321 auto-tuning temperature controllers with sensitivity better than ±0.1 K. The absorption spectra of the films were measured at room temperature by Perkin-Elmer Lambda 2SUV/Vis Spectrometer with 190–1100 nm wavelength range using non-polarized light.

3. Results and discussion

Fig. 3 shows the XRD pattern of CdS thin films annealed at 300 °C for 1 h in vacuum. The diffraction pattern of the CdS thin films corresponds to the zinc-blend type with a preferential orientation of (1 1 1) planes. No diffraction peaks of CdO or other impurity phases were found in these samples. The lattice parameter, *a*, was calculated from the position of the XRD (1 1 1) peak. The calculated α value was found to be 0.582 nm. We obtained the dislocation density for Cu/CdS/SnO_2/In–Ga structure as 4.01×10^{14} lines/m^2 [20]. Also, XRD pattern of SnO_2 coated glass substrate was measured and was observed amorphous structure.

In the case of pure TE theory ($V \geq 3\,kT/q$), the relation between the applied forward bias voltage *V* and the current *I* can be expressed as [14,15,37,38]:

$$I_{TE} = I_o \left[\exp\left(\frac{qV}{kT}\right) - 1 \right] \quad (1a)$$

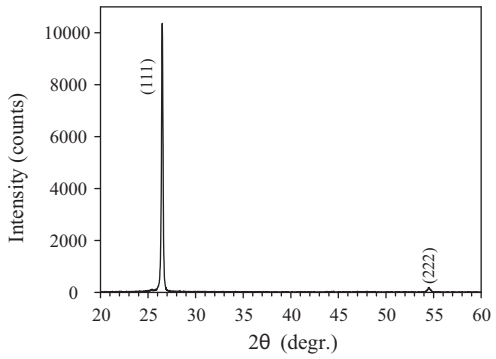

Fig. 3. XRD patterns of CdS thin films.

When SBD with a series resistance R_s and the value of n is greater than unity, Eq. (1) can be modified as [14,39]:

$$I_{TE} = I_o \left[\exp\left(\frac{q(V - IR_s)}{nkT}\right)\right]\left\{1 - \exp\left[\frac{q(V - IR_s)}{kT}\right]\right\} \quad (1b)$$

where the terms of the IR_s is voltage drop across series resistance of structure, n is the ideality factor and I_o ($=I_{TEo}$) is the reverse-saturation current. The ideality factor (n) is introduced to take the deviation of the experimental I–V data from the ideal TE theory into account. From Eq. (1b), the value of n can be calculated from the slope of the straight line region of the forward bias ln(I)–V plot for each temperature and can be written as:

$$n = \frac{q}{kT}\frac{d(V - IR_s)}{d(\ln I)} \quad (1c)$$

Similarly, the value of I_o can be derived from the straight line region of the forward bias ln(I)–V plot at a zero bias for each temperature and is given by:

$$I_o = A^* A T^2 \exp\left(\frac{-q\Phi_{Bo}}{kT}\right) \quad (2a)$$

where the quantities A^*, A, and Φ_{Bo} are the effective Richardson constant which is equal to 23 A/cm^2 K^2 for n-type CdS, the area of diode, and the zero-bias barrier height, respectively. Once I_o is determined, Φ_{Bo} is obtained by rewriting Eq. (2a) as:

$$\Phi_{Bo} = \frac{kT}{q}\ln\left[\frac{AA^*T^2}{I_o}\right] \quad (2b)$$

In practice, the situation is different from the ideal case (pure TE and modified TE) especially at low temperatures and with high doped semiconductors. Then, the total current can be rewritten as [11]:

$$\begin{aligned} I_{total} &= I_{TE} + I_{GR} + I_{Tun} + I_{LE} \\ I_{total} &= I_{TEo}\left\{\exp\left(\frac{q(V - IR_s)}{kT}\right) - 1\right\} \\ &\quad + I_{GRo}\left\{\exp\left(\frac{q(V - IR_s)}{2kT}\right) - 1\right\} \\ &\quad + I_{Tuno}\left\{\exp\left(\frac{q(V - IR_s)}{E_o}\right) - 1\right\} + \frac{V - IR_s}{R_{sh}} \end{aligned} \quad (3)$$

where the first term is the Thermionic emission (TE) current as given in Eq. (1b) and I_{TEo} is given in Eq. (2a). Second term is the generation-recombination (GR) current and I_{GRo} is given by:

$$I_{GRo} = \frac{qn_i W_D}{2\tau} \quad (3a)$$

where W_D is the thickness of the semiconductor depletion region, τ is the electron effective life time within the depletion region and n_i is the intrinsic electron concentration. Third term is the tunneling current through the barrier. Here, I_{Tuno} is the tunneling saturation current and E_o is the parameter dependent on the barrier transparency. E_o can be defined as [14,15,20,38]:

$$E_o = E_{oo}\coth\left(\frac{E_{oo}}{kT}\right) \quad (3b)$$

where E_{oo} is the characteristics tunneling energy that is related to the tunnel effect transmission probability and is given by:

$$E_{oo} = \frac{qh}{4\pi}\left(\frac{N_D}{m_e^*\varepsilon_s}\right)^{1/2} \quad (3c)$$

where m_e^* is the electron effective mass, h is the Planck' s constant and N_D is the carrier (donor) concentration. The fourth term is leakage current and the R_{sh} is shunt resistance of structure. Choosing the proper saturation currents I_{TEo}, I_{GRo}, I_{Tuno}, the tunneling parameter E_o and resistances R_s and R_{sh} allows us to fit the experimental forward bias I–V plots in a wide range of applied biases and at various temperatures. In general, at higher temperature the TE and the GR are dominant whereas the tunneling (TFE and FE) and leakage currents become more significant at lower temperatures and for higher doped materials [40–42].

Fig. 4(a) shows a set of semi-logarithmic forward and reverse bias I–V characteristics of a Cu/CdS/SnO_2/In–Ga structure measured in the temperature range of 130–325 K (the inset shows schematic layering in the diode and the contacts for I–V data). As can be seen in Fig. 4(a), the ln$I$–V plots of Cu/CdS/SnO_2/In–Ga structure depict increasingly linear behavior in the intermediate bias voltages (~0.1 V ≤ V ≤ 0.7 V) over several of current but deviated from the linearity because of the effect of R_s. However, it can be seen that the current rises slowly with the applied reverse bias and does not show any effect of saturation for each temperature. Such behavior of the lack of saturation under reverse bias can be commonly explained in terms of image force lowering of BH and the existence of a native or deposited interfacial layer between the metal and semiconductor [14,15,37]. The experimental values of the ideality factor n, I_o and Φ_{Bo} determined from Eqs. (1c), (2a) and (2b), respectively, for each temperature and were given in Table 1. As can be seen in Table 1, we found n, I_o and Φ_{Bo} values ranging from 8.98, 7.6×10^{-8} A and 0.29 eV (at 130 K) to 3.42, 7.6×10^{-7} A and 0.72 eV (at 325 K), respectively. As can be seen in Table 1, while n decreases, Φ_{Bo} increases with the increasing temperature. The values of Φ_{Bo} increase with the increasing temperature such that there is a positive coefficient that is in contrast to the negative dependence measurements by Crowell and Rideout [43] in silicon Schottky diodes and Mead and Spitzer [44] in InAs and InSb, which closely follow the charge in the forbidden energy band gap (E_g) with temperature. Such behavior of Φ_{Bo} and n obviously implies a deviation from TE mechanism.

Table 1
Temperature dependent values of various parameters determined from forward bias I–V characteristics of Cu/CdS/SnO_2/In–Ga structure.

T (K)	I_o (A)	n	Φ_{Bo} (eV)	nT (K)	R_s (at 1.4 V) (Ω)	R_{sh} (at −1.4 V) (Ω)
130	7.60×10^{-8}	8.98	0.29	1166.89	1026	109,555
150	1.01×10^{-7}	7.32	0.34	1097.94	746	81,425
200	1.86×10^{-7}	5.94	0.45	1189.15	645	60,862
230	2.63×10^{-7}	4.79	0.52	1102.11	513	53,892
270	4.05×10^{-7}	4.20	0.60	1134.46	320	48,584
300	5.69×10^{-7}	4.07	0.67	1221.00	221	43,102
325	7.60×10^{-7}	3.42	0.72	1110.56	150	39,142

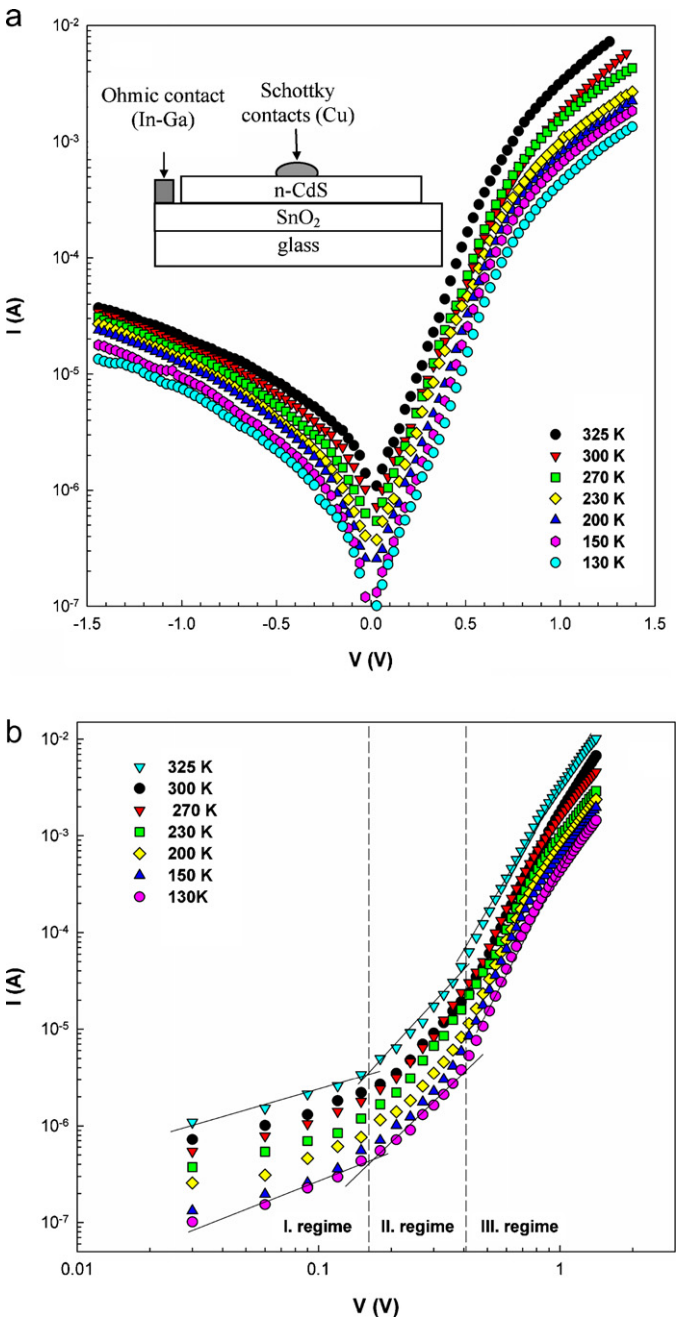

Fig. 4. (a) The semi-logarithmic forward and reverse bias (the inset given schematic layering in the diode and the contacts for *I–V* data) and (b) double-logarithmic forward bias *I–V* characteristics of the Cu/CdS/SnO_2/In–Ga structure at various temperatures.

In order to interpret the current-transport mechanisms such as TE, space charge limited current (SCLC) and trap-charge limited current (TCLC) mechanisms, double logarithmic forward bias ln*I*–ln*V* plots for the Cu/CdS/SnO_2/In–Ga structure were given in Fig. 4(b) for each temperature level. As can be seen in Fig. 4(b), the forward bias ln*I*–ln*V* plots have three distinct linear regions with different slopes for each temperature, indicating different conduction mechanisms. If there exist deep traps at the M/S interface, the charge conduction profile is modified and these modifications affect the slopes of the forward bias *I–V* characteristics. At low voltages (I. regime), the current-transport mechanism for the sample exhibits an ohmic behavior, that is, the current is directly proportional to applied bias voltage [10,45–47]. This behavior can be attributed to the superiority of bulk generated current in the film to the injected free carrier generated current [47–49]. At intermediate voltages (II. regime), where the slopes of the plots are larger than two, such behavior of the plot can be evaluated as an indication of TCLC mechanism with an exponent trap distribution [47]. In strong forward bias region (III. regime), because of the strong electron injection, the electrons escape from the traps and contribute to SCLC [47–52].

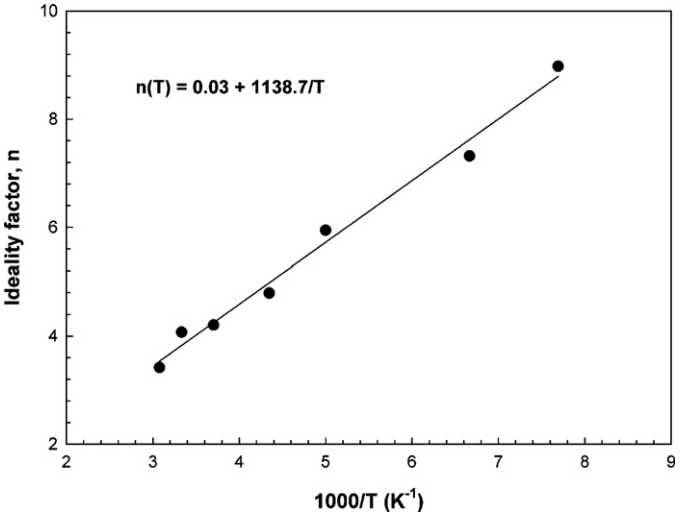

Fig. 5. The plot of *n* vs 1000/*T* for the Cu/CdS/SnO_2/In–Ga structure.

The change in *n* with temperature is seen in Table 1, and *n* was found to change linearly (Fig. 5) with the inverse temperature as:

$$n(T) = n_o + \frac{T_o}{T} \quad (4)$$

where the n_o and T_o are constants which were found as 0.03 and 1138.7 K, respectively. As shown in Fig. 3, the value of *n* decreases with the increasing temperature and changes linearly with the inverse temperature (1/T). Such behavior of *n* can be described as the "To anomaly or effect". The other reason such temperature dependence of *n* could be attributed to the inhomogeneties of the SBH [53]. Consequently, the experimental results reveal an abnormal increase in the Φ_{Bo} and a decrease in the n with temperature that leads to non-linearity in the conventional Richardson plot of $\ln(I_o/T^2)$ vs q/kT (Fig. 5). As can be seen in Table 1, the values of *nT* are more or less constant. Therefore, TFE mechanism can also be ruled out in whole temperature region. On the other hand, there is a correlation between the experimental and the theoretical plots (nkT/q) vs (kT/q) for the sample seen in Fig. 6. TFE is unlikely an

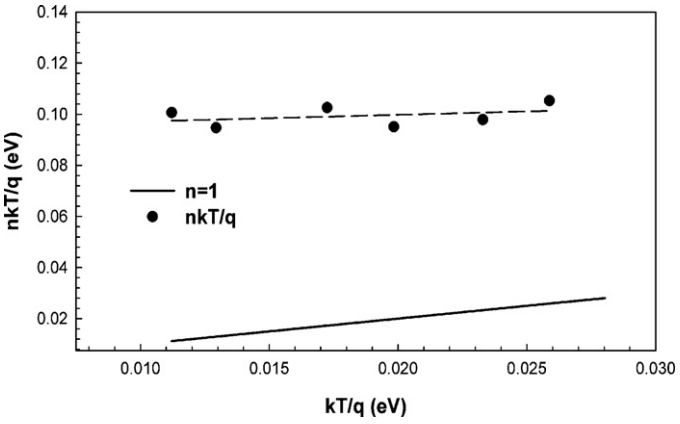

Fig. 6. Experimentally and theoretically found tunneling current parameter (nkT/q) vs (kT/q) for the Cu/CdS/SnO_2/In–Ga structure.

active mechanism, since it would be predominant only at quite low temperatures for the semiconductor material having high doping concentrations, which is not the case for the CdS substrate used in the present study ($n = 1.8 \times 10^{13}$ cm^{-3}). The minority carrier injection mechanism is also unlike for our sample in the intermediate bias region, since it would be expected to be significant only for the samples having very high effective BH value near to the band gap of semiconductor and very low reverse saturation current with temperature independent diode quality factor having the value of almost unity ($n = 1$) [19,54]. The range of the n values (8.98 at 130 K and 3.42 at 325 K) and the temperature dependent behavior suggest a conduction mechanism controlled by TFE [19–21,53]. The large values of n especially at low temperatures may be attributed to the effects of the bias voltage drop across the interfacial layer, the particular distribution of interface and fluctuations of barrier height at M/S interface [19,21,47,55].

For the determination of the barrier height, one may also make use of the Richardson plot of the saturation current Eq. (2a) can be written as:

$$\ln(I_o/T^2) = \ln(AA^*) - \left(\frac{q\Phi_{Bo}}{kT}\right) \quad (5)$$

The dependence of $\ln(I_o/T^2)$ vs q/kT is given in Fig. 7. The conventional energy variation of $\ln(I_o/T^2)$ vs q/kT plot is found to be non-linear in the temperature range measured. The non-linearity of the $\ln(I_o/T^2)$ vs q/kT plot is caused by temperature dependence of BH and n. However, the experimental data are shown to fit asymptotically with almost a straight line above 270 K, yielding an activation energy of 0.02 eV, and the Richardson constant (A^*) value of 1.68×10^{-9} A/cm^2 K^2 is determined from intercept at the ordinate of this experimental plot, which is much lower than the known value of 23 A/cm^2 K^2 for n type CdS. This deviation in A^* may be due to the spatial inhomogeneous BH and potential fluctuation at the interface that consist of low and high barrier areas [37,56]. Furthermore, the value of A^* obtained from I–V characteristics as a function of temperature may be affected by the lateral inhomogeneity of the barrier.

The saturation current was found to change linearly with the temperature (Fig. 7). As can be seen in Fig. 8, the slope of $\ln(I_o)$ vs T plot is almost temperature independent with a value of approximately 10.109 V^{-1}. Also, the reverse saturation current depends on temperature (Fig. 7), and diode ideality factor was found to be strongly dependent on temperature with $n > 1$. According to the tunneling model, which was developed for Schottky barriers, the band bending works as a barrier for carriers tunneling into interface states or dislocations, where various traps may be involved in multi-tunneling steps [20,42,57]. Thermally activated carriers make (step-wise) tunneling into the interface states possible. Therefore, it seems that trap assisted multistep tunneling may be the mechanism that dominates the forward bias I–V characteristics in this voltage and temperature range for Cu/CdS/SnO$_2$/In–Ga structures. The forward I–V relationship for this mechanism is given [42,57] by

$$I(V, T) = I_o(T)\exp(AV) \quad (6)$$

where I_o is a constant proportional to the density of traps of appropriate energy in the CdS space charge region and A is a constant calculated from tunneling theory ($A = d\ln(I)/dV$). As a results, the analysis of the temperature dependent forward bias I–V data of our structures indicated that there was no single current-transport mechanism being predominant in this region of applied bias voltage. In addition, analysis of the data in this region was difficult since the I–V characteristics were extremely sensitive to the shunt and series resistance of structure which are also temperature dependent [19,38].

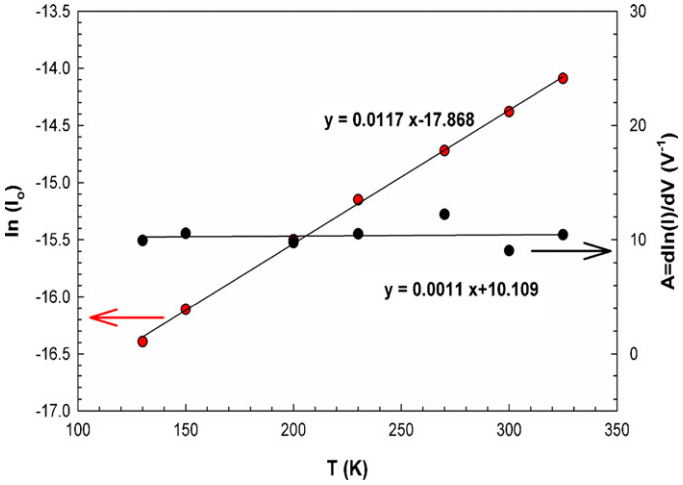

Fig. 8. The temperature dependence of I_o and A for the Cu/CdS/SnO$_2$/In–Ga structure.

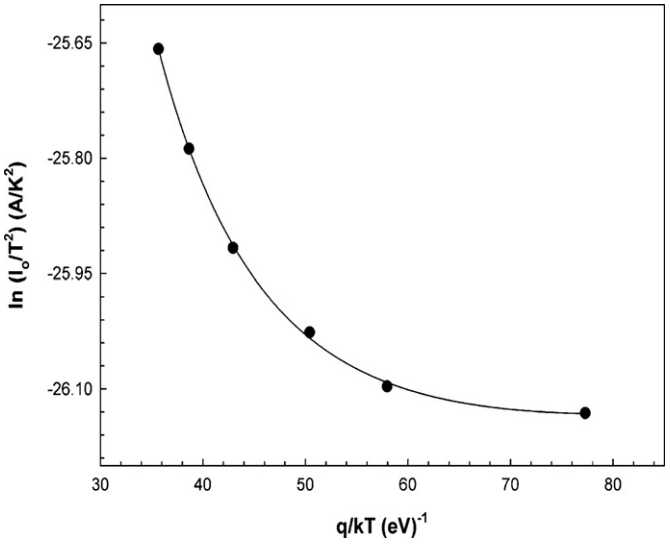

Fig. 7. Richardson plot of the $\ln(I_o/T^2)$ vs q/kT for the Cu/CdS/SnO$_2$/In–Ga structure.

The series resistance (R_s) and shunt resistance (R_{sh}) are determined from the structure resistance (R_i) versus applied bias voltage (V_i) plot determined from the forward and reverse bias I–V characteristics by using Ohm's law ($R_i = dV_i/dI_i$) and they were given in Fig. 9. It was observed that at sufficiently high forward bias voltage the structure's resistance values approach to a constant value which corresponds to the R_s value for SnO$_2$/CdS/Cu structure. Similarly, also at sufficiently high reverse bias voltage, the structure's resistance values reach to constant value, which is equal to structure's shunt resistance (R_{sh}). It is clear that the magnitude of the resistance values decreases with the increasing temperature according to literature [38]. It may be associated to the increase in the number or density of the free charge carriers, either by bond breaking or de-trapping mechanism [29,58]. The values of R_s and R_{sh} obtained from I–V data at 1.4 and −1.4 V, respectively, were also given in Table 1. As can be seen in Table 1, both resistance values decrease with the increasing temperature according to literature. Also, the values of R_s decrease with the increasing applied bias voltage (inset of Fig. 9).

In order to obtain information about the band gap, transmission measurements were carried out in the range of 190 and 1100 nm. A plot of optical transmittance spectra of the CdS films as a function of wavelength is shown in Fig. 10. The maximum transmission of the CdS thin films was above 80%. Also, the optical transmittance

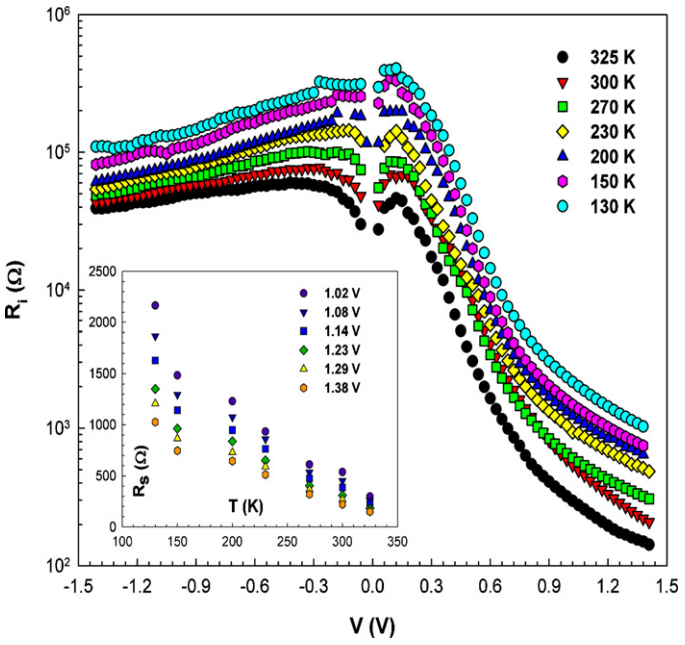

Fig. 9. The plot of the structure resistance vs applied bias voltage as a function of temperature for the Cu/CdS/SnO_2/In–Ga structure.

spectra of CdS on SnO_2 coated glass substrate were measured and interference fringe in the spectrum was observed. The existence of interference fringe pattern shows that samples have a smooth surface and uniform thickness [59]. Furthermore, the optical band gap energy E_g from the absorption spectra measured in the range of 190–1100 nm were calculated by using the dependence of the absorption coefficient (α) on the photon energy;

$$(\alpha h\nu) = A^*(h\nu - E_g)^{1/2} \quad (7)$$

where E_g is the optical band gap of thin films and A^* is a constant having the numerical values of $2 \times 10^4\ \mathrm{cm}^{-1}(\mathrm{eV})^{-1/2}$ when α is expressed in cm^{-1}, $h\nu$ and E_g are in electron volt (eV). An energy gap of 2.42 eV is obtained by extrapolating the linear part of the $(\alpha h\nu)^2$ vs $(h\nu)$, as typically shown in the inset of Fig. 10. This value is found to be in a good agreement with the literature [5].

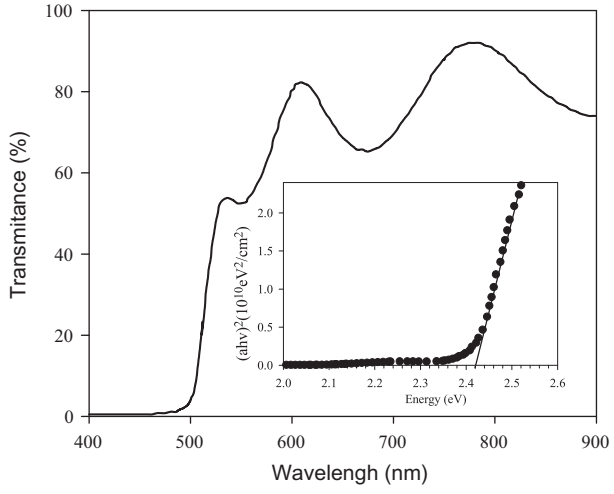

Fig. 10. Optical transmission spectra for CdS thin films. Inset shows the optical band gap of sample as estimated by Tauc's plot.

4. Conclusions

The forward bias *I–V* characteristics of Cu/CdS/SnO_2/In–Ga structure have been investigated in the temperature range of 130–325 K. From the slope of each plot, the ideality factor values of the structure were found to be strongly temperature dependent and changed linearly with the inverse of temperature ($1/T$). The forward bias current I is found to be proportional to $I_o(T)\exp(AV)$, where A is the slope of $\ln(I)$–V plot and almost independent of the applied bias voltage and temperature, and $I_o(T)$ is relatively a weak function of temperature. Also, the $\ln I_o$ values extracted from the forward bias *I–V* data showed a fairly linear behavior with the temperature. These results show that the charge transport mechanism in the whole temperature range in the forward-biased Cu/CdS/SnO_2/In–Ga structure was performed by the tunneling mechanism among the interface states or dislocations intersecting the space-charge region. The dislocation density value (DD) that was obtained from the X-ray diffraction (XRD) measurements is 4.01×10^{14} lines/m^2. This data shows that the current flows manifest a tunneling character, even at high temperature. A more detailed comparative study involving the traps in the depletion layer of CdS is required to understand the effects governing the predominant carrier transport mechanism in these structures. In addition, voltage dependent values of R_s and R_{sh} decrease with the increasing temperature in consistency with the literature.

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